

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Karl Joseph Bois et al.

Confirmation No.:

Application No.:

Examiner:

Filing Date: 02/19/04

Group Art Unit:

Title: Printed Circuit Board Substrate and Method for Constructing Same

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

- (X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)
- () under 37 CFR 1.97(c) together with either a:
() Statement under 37 CFR 1.97(e), or
() a \$180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)
- () under 37 CFR 1.97 (d) together with a:
() Statement under 37 CFR 1.97(e)(1) or (2), and
() a \$180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

() A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individual(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

* Express Mail* label no. **EV386626693US**

Date of Deposit **02/19/04**

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By

Typed Name: **Shreen K. Danamraj**

Respectfully submitted,

Karl Joseph Bois et al.

By

Shreen K. Danamraj

Attorney/Agent for Applicant(s)
Reg. No. **41,696**

Date: **02/19/04**

PATENT APPLICATION

Sheet 1 of 1

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
	200315309-1		
	APPLICANT		
	Karl Joseph Bois et al.		
	FILING DATE	GROUP	
	02/19/04		

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	4,747,897	05-31-1988	Johnson	
	1B	6,353,997	03-12-2002	Su	
	1C	6,387,205	05-14-2002	Appelt et al.	
	1D	2002/0125044	09-12-2002	Johnson	
	1E				
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

1Q	"Printed Wiring Board Products"; Hitachi Chemical Co. America, Ltd.; 2 pages; undated.
1R	PARTANGEL, NARAYANAN S.; Master's Thesis; "The Relationship Between Process and Manufacturing Plant Performance: A Goal Programming Data Envelopment Analysis Approach"; Chapter 5; Digital Library and Archives; Pages 47-56; September 17, 1999
1S	"A Low Loss Dielectric for High Frequency HDI Substrates and PCBs"; Microwave Journal; 2 pages; December 2000

EXAMINER	DATE CONSIDERED
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